WHAT IS CLAIMED IS:

1. An LCD device, comprising:

an insulating substrate;

a gate line disposed on the insulating substrate;

a first data line disposed perpendicular to the gate line and separated from the gate line;

a second data line disposed crossing the gate line on a same line as the first data line;

a thin film transistor disposed substantially at a crossing point of the gate line and the second data line;

an active layer disposed below the second data line, a source electrode, and a drain electrode of the thin film transistor;

a third data line disposed perpendicular to the gate line to define a pixel region to electrically connect the first and second data lines with each other; and

a pixel electrode disposal in the pixel region.

2. The LCD device according to claim 1, wherein the first data line is formed on the same layer as the gate line with the same material as the gate line.

3. The LCD device according to claim 1, wherein the gate line and the first data line are formed of at least one of chrome (Cr), aluminum (Al), aluminum alloy (AlNd), tantalum (Ta) and molybdenum (Mo).

4. The LCD device according to claim 1, wherein the first data line is formed adjacent to the pixel electrode.

5. The LCD device according to claim 1, further comprising a passivation layer formed over an entire surface of the insulating layer including the second data line.

6. The LCD device according to claim 5, wherein the passivation layer includes first, second and third contact holes respectively formed on both sides of the first data line, on both sides of the second data line, and on a predetermined portion of the drain electrode.

7. The LCD device according to claim 6, wherein the third data line electrically connects the first and second data lines to each other through the first and second contact holes.

8. The LCD device according to claim 1, wherein the thin film transistor includes:

a source electrode protruding from the second data line;

a drain electrode being apart from the source electrode; and

a gate electrode extending from the gate line.

9. The LCD device according to claim 8, wherein the source electrode is partially overlapped on a first side of the gate electrode to define a 'C'-shaped groove.

10. The LCD device according to claim 8, wherein the drain electrode is partially overlapped on a second side of the gate electrode to be spaced apart from the source electrode such that the drain electrode is disposed inside the 'C'-shaped groove.

11. The LCD device according to claim 8, further comprising an ohmic contact layer on the active layer corresponding to the second data line, the source electrode, and the drain electrode except the channel region.

12. The LCD device according to claim 1, wherein the pixel electrode is formed on the same layer as the third data line.

13. The LCD device according to claim 12, wherein the pixel electrode and the third data line are formed of a transparent electrode material such as Indium-Tin-Oxide (ITO), Tin-Oxide (TO) or Indium-Zinc-Oxide (IZO).

14. The LCD device according to claim 1, wherein the second data line is formed by sequentially depositing an amorphous silicon layer, an n^+ amorphous silicon layer and a metal layer.

15. A method for manufacturing an LCD device, comprising the steps of:

forming a gate line and a first data line on an insulating substrate, the gate line having a gate electrode, the first data line being perpendicular to the gate line and spaced apart from the gate line;

sequentially depositing a semiconductor layer and a conductive layer after forming a gate insulating layer on an entire surface of the insulating substrate including the gate line and the first data line;

forming a second data line on the same layer as the first data line by patterning the semiconductor layer and the metal layer, the second data line having source/drain electrodes perpendicular to the gate line;

forming a third data line on the first and second data lines to electrically connect the first and second data lines with each other, thereby defining a pixel region; and

forming a pixel electrode in the pixel region.

16. The method according to claim 15, wherein the first data line is formed on the same layer as the gate line at the same time.

17. The method according to claim 15, wherein the gate line and the first data line are formed of at least one conductive metal layer of chrome (Cr), aluminum (Al,) aluminum alloy (AlNd), tantalum (Ta) and molybdenum (Mo).

18. The method according to claim 15, wherein the first data line is formed adjacent to the pixel electrode.

19. The method according to claim 15, wherein the step for forming the second data line having the source/drain electrodes includes the steps of:

sequentially depositing the first and second semiconductor layers and the conductive layer on the gate insulating layer;

patterning a photoresist pattern on the conductive layer using a half-tone mask having a diffraction exposing portion above the channel region;

etching the conductive layer and the first and second semiconductor layers using the photoresist pattern;

ashing the photoresist pattern to expose the conductive layer above the channel region;

forming the separated source and drain electrodes, and the second data line by etching the conductive layer and the second semiconductor layer to expose the first semiconductor layer of the channel region while simultaneously forming an ohmic contact layer on the active layer except the channel region; and

removing the photoresist pattern.

20. The method according to claim 19, wherein the source electrode is partially overlapped on a first side of the gate electrode to define a 'C'-shaped groove.

21. The method according to claim 19, wherein the drain electrode is partially overlapped on a second side of the gate electrode to be spaced apart from the source electrode such that the drain electrode is disposed inside the 'C'-shaped groove.

22. The method according to claim 15, further comprising a step for forming a passivation layer formed over an entire surface of the insulating substrate including the second data line.

23. The method according to claim 22, wherein the passivation layer is formed of at least one of an inorganic insulating layer including silicon nitride or silicon oxide, and an organic insulating layer including BenzocycloButene (BCB) or acrylic resin.

24. The method according to claim 22, wherein the passivation layer includes first, second and third contact holes respectively formed on both sides of the first data line, on both sides of the second data line, and on a predetermined portion of the drain electrode.

25. The method according to claim 24, wherein the third data line electrically connects the first and second data lines to each other through the first and second contact holes.

26. The method according to claim 15, wherein the pixel electrode is formed on the same layer as the third data line at the same time.

27. The method according to claim 15, wherein the pixel electrode and the third data line are formed of a transparent electrode material such as Indium-Tin-Oxide (ITO), Tin-Oxide (TO) or Indium-Zinc-Oxide (IZO).